

FIG. 1

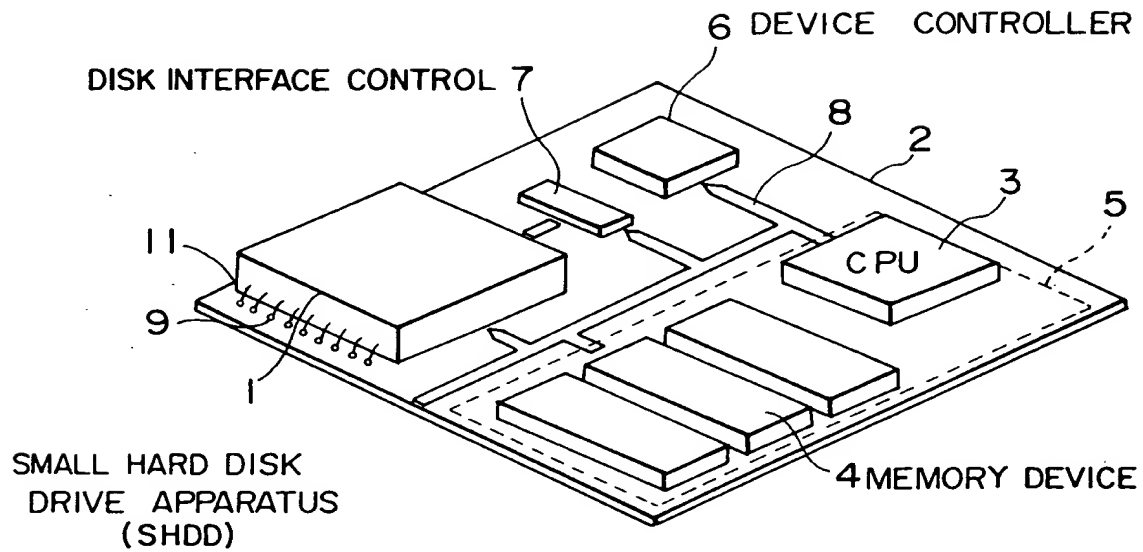
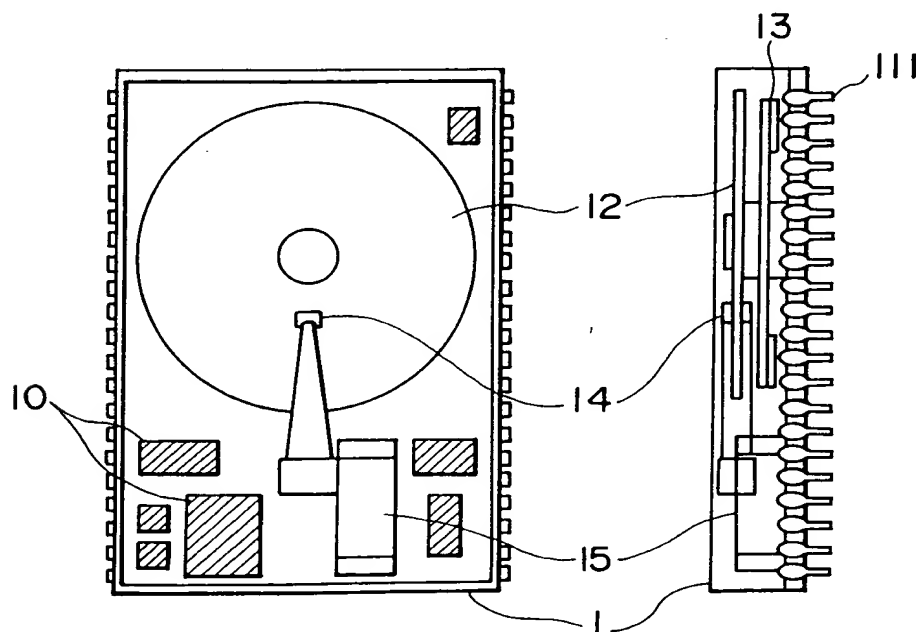


FIG. 2



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FIG. 3

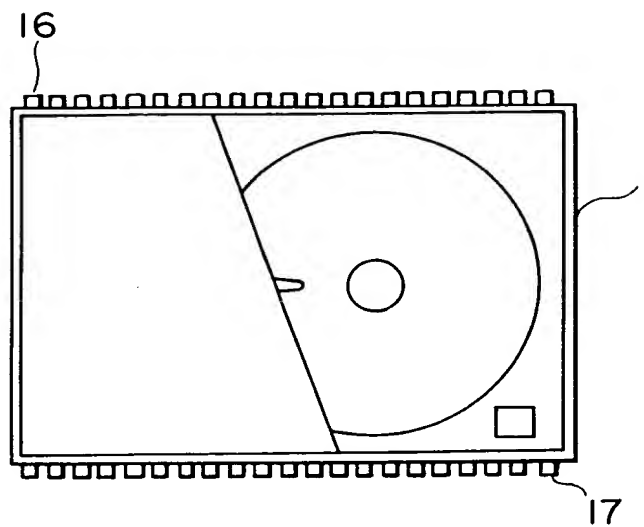
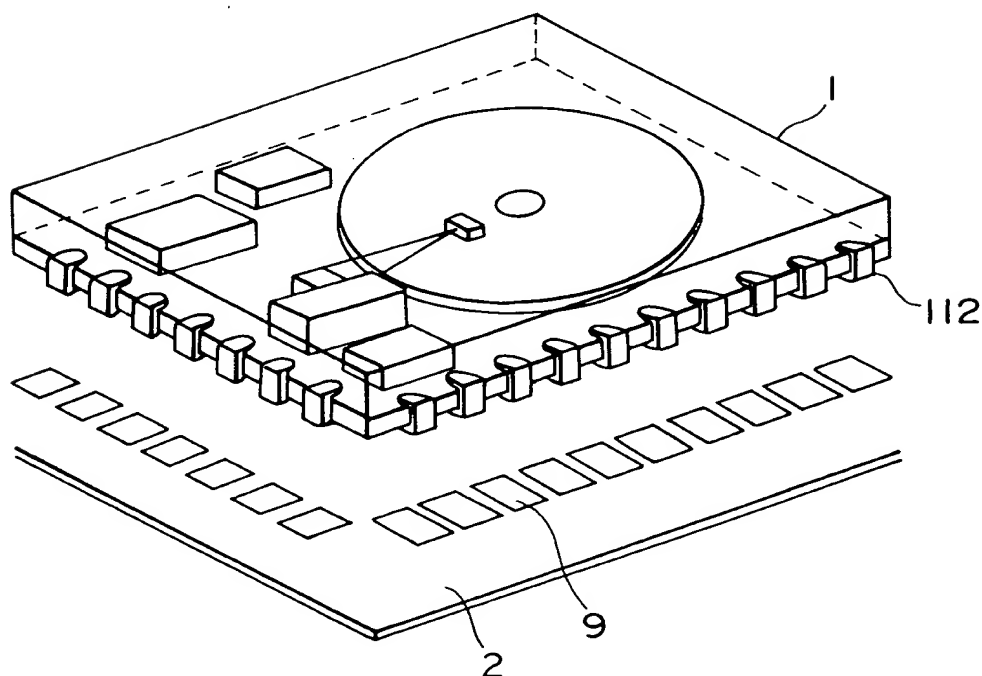


FIG. 4



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FIG. 5

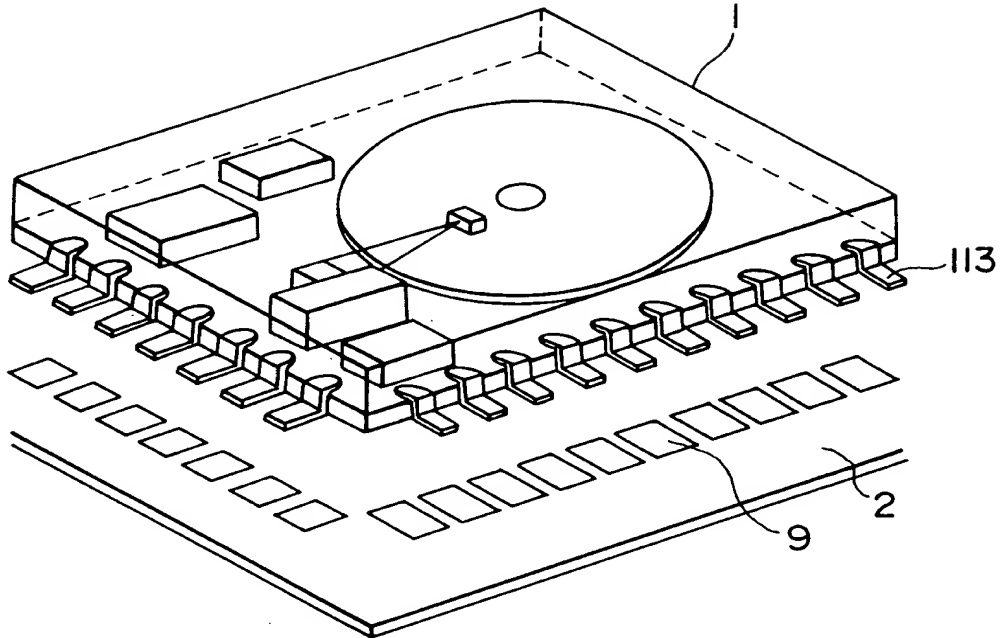
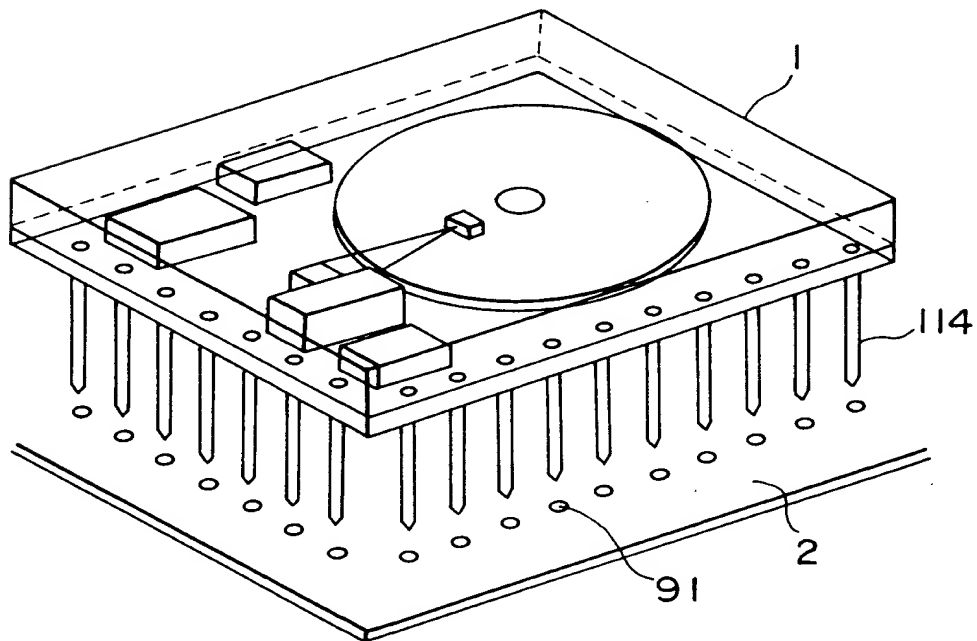


FIG. 6



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RV		
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FIG. 7

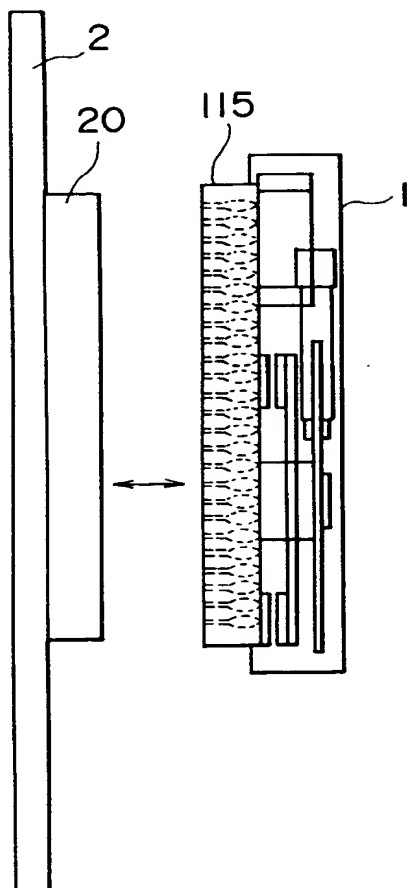


FIG. 8

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
01	GND	02	D B 0
03	GND	04	D B 1
05	GND	06	D B 2
07	GND	08	D B 3
09	GND	10	D B 4
11	GND	12	D B 5
13	GND	14	D B 6
15	GND	16	D B 7
17	GND	18	D B P
19	GND	20	GND
21	GND	22	GND
23	GND	24	GND
25	OPEN	26	TERM PWR
27	GND	28	GND
29	GND	30	GND
31	GND	32	ATN
33	GND	34	GND
35	GND	36	BSY
37	GND	38	ACK
39	GND	40	RST
41	GND	42	MSG
43	GND	44	SEL
45	GND	46	C / D
47	GND	48	REQ
49	GND	50	I / O

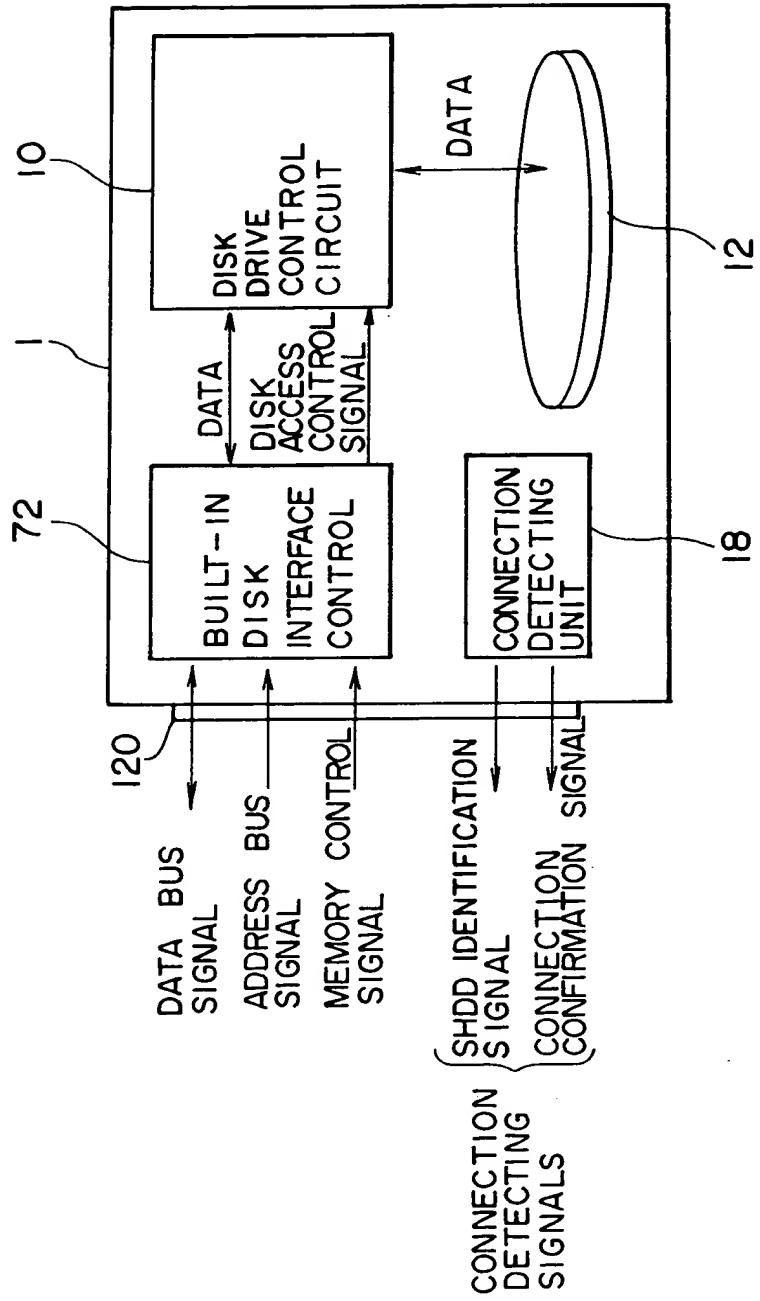
FIG. 9

PIN NO	SIGNAL NAME	PIN NO	SIGNAL NAME
01	A T N	02	D B 0
03	B S Y	04	D B 1
05	A C K	06	D B 2
07	R S T	08	D B 3
09	M S G	10	D B 4
11	S E L	12	D B 5
13	C / D	14	D B 6
15	R E Q	16	D B 7
17	I / O	18	D B P

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BY	CLASS	SUBCLASS
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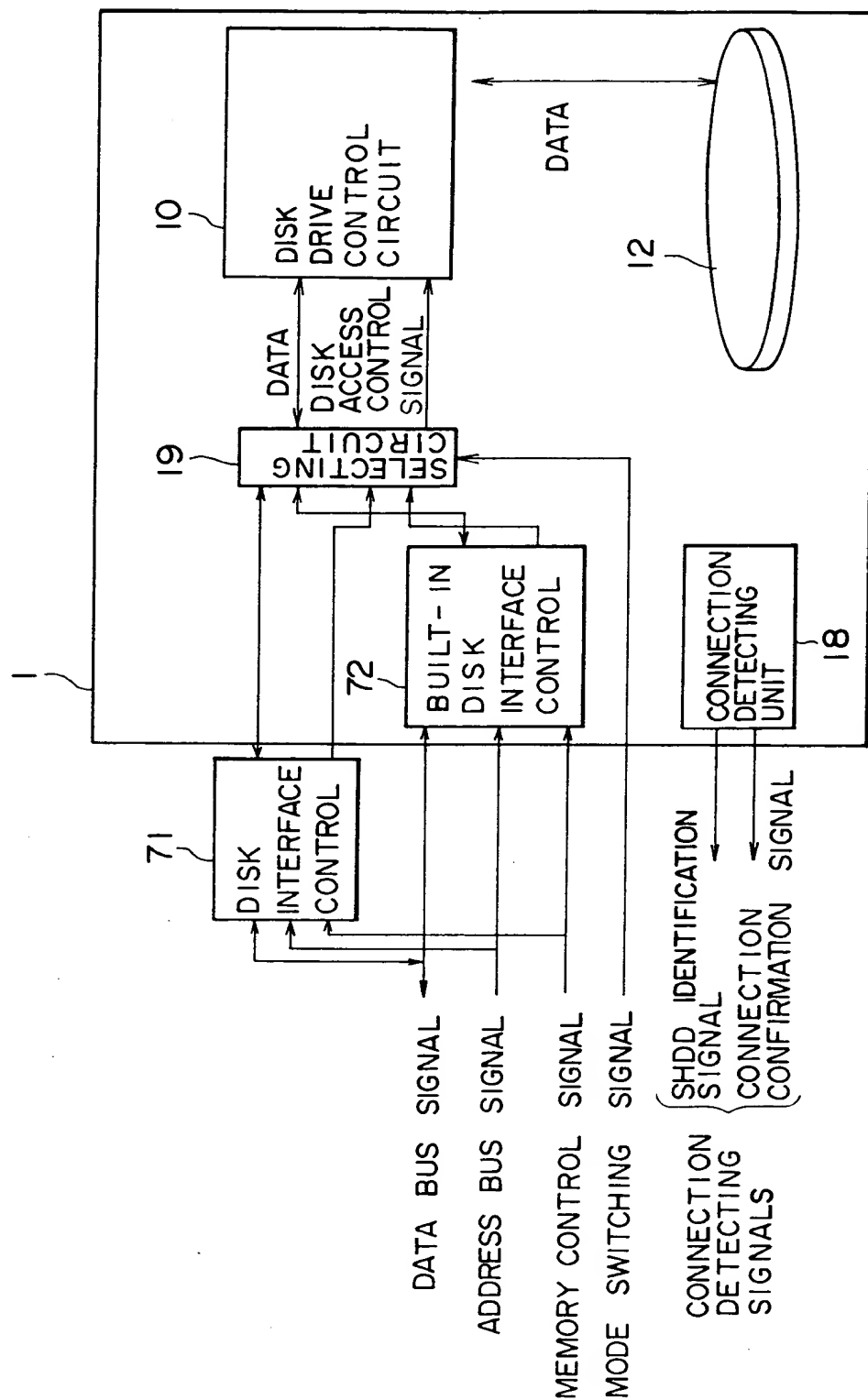
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FIG. 10



APPROVED	C. S. FIG
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FIG. 13



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FIG. 15

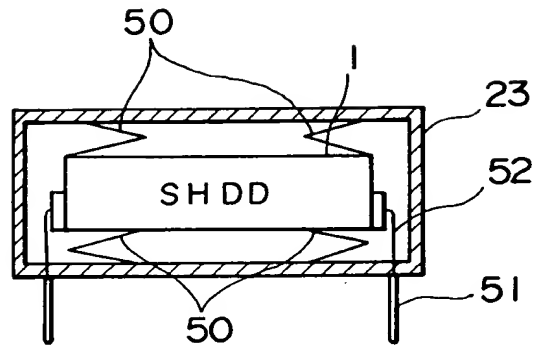
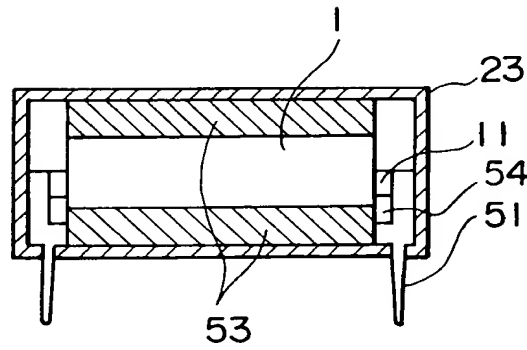


FIG. 16



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APPROVED	C. C. FIG	
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FIG. 17

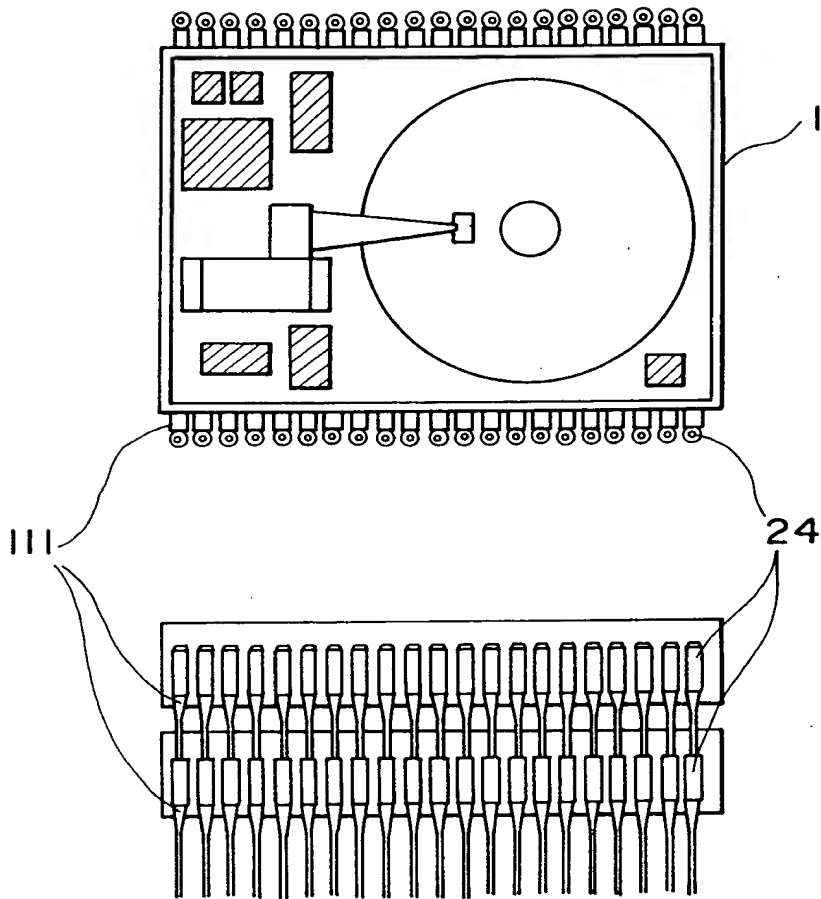
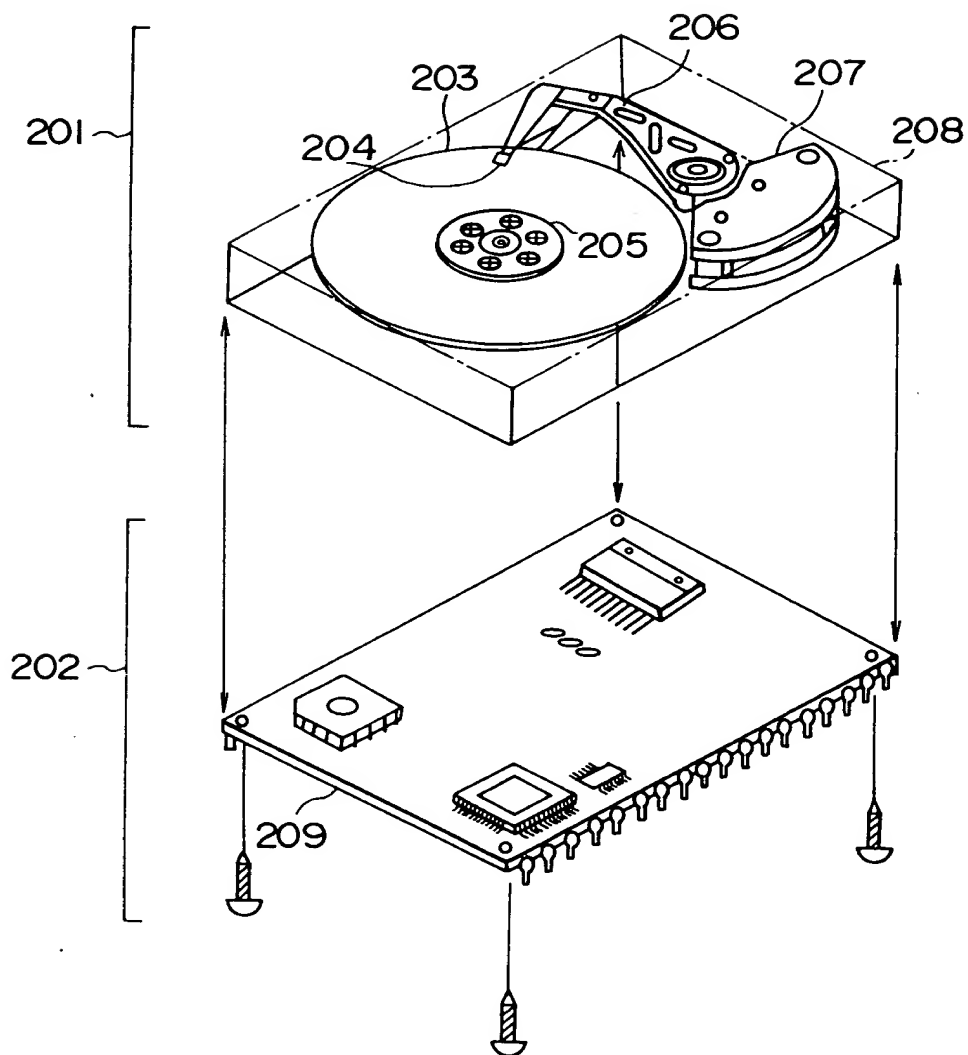


FIG. 17

APPROVER	C. C. FIG.	
RV	CLASS	RECLASS
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FIG. 18

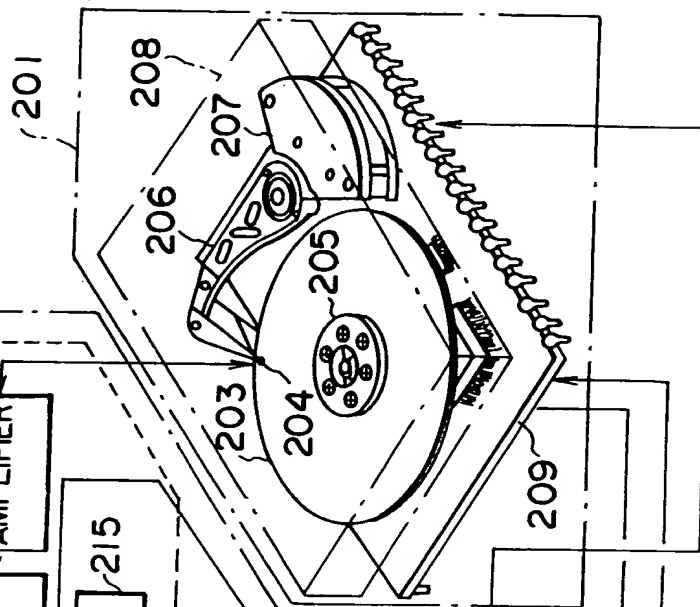


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The diagram illustrates the system architecture of a hard disk drive. An **EXTERNAL HOST** (212) is connected to the drive's control logic. The drive's internal components are organized into several functional blocks:

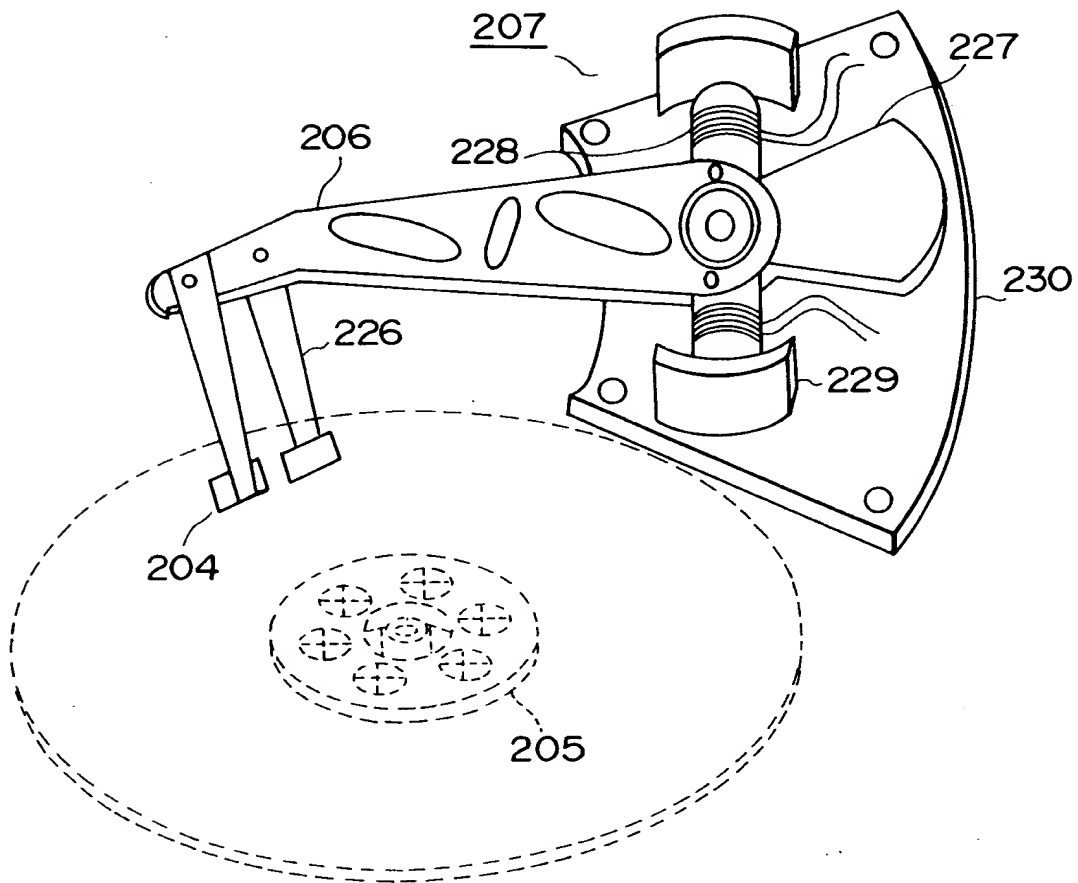
- Control and Data Path (211):** Includes the **SCSI CONTROLLER** (222), **BUFFER RAM** (224), **HDC** (223), and **CPU** (225). The SCSI controller and buffer RAM are connected to the external host. The CPU is connected to the SCSI controller, HDC, and the write clock generating circuit.
- Signal Processing (210):** Contains the **WRITE CLOCK GENERATING CIRCUIT** (221), **HEAD POSITIONING CONTROL CIRCUIT** (218), **POSITIONAL SIGNAL GENERATING CIRCUIT** (217), **MOTOR DRIVER** (219), and **SPINDLE MOTOR CONTROL/DRIVER** (220). The CPU provides control signals to the write clock and head positioning circuits. The head positioning circuit controls the motor driver, which in turn controls the spindle motor control/driver.
- Data and Error Correction (214):** Includes the **FN CODE / CIRCUIT** (216), **DATA SEPARATOR** (215), **WAVEFORM SHAPING CIRCUIT (EQUALIZER)** (213), and **R/W AMPLIFIER** (213). The data separator is connected to the SCSI controller and the waveform shaping circuit. The waveform shaping circuit is connected to the R/W amplifier.
- Head and Disk Assembly (201):** Shows a cross-section of the disk head and disk. The **HEAD** (204) is positioned over the **DISK** (205). The **SLIDE** (206) and **ACTUATOR** (207) are shown. The **SPINDLE MOTOR** (208) is at the center. The **WIRE** (209) is connected to the disk head.

Connections are shown between the external host and the SCSI controller, and between the CPU and the write clock and head positioning circuits. The head positioning circuit controls the motor driver, which in turn controls the spindle motor control/driver. The data separator is connected to the SCSI controller and the waveform shaping circuit. The waveform shaping circuit is connected to the R/W amplifier.



APPROVER	C. J. FIG.	
rv	CLASS	SUBCLASS
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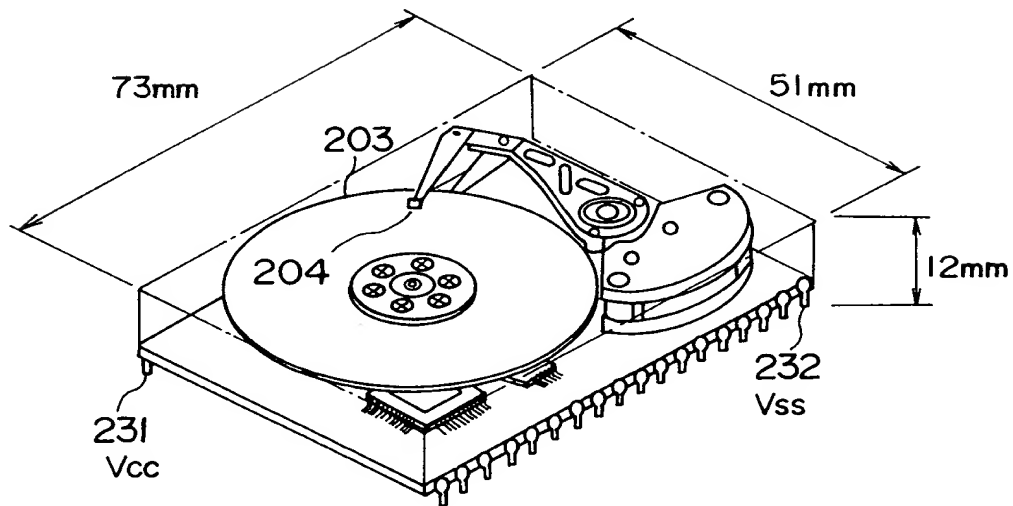
FIG. 21



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APPROVED	C.C. FIG.	
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FIG. 22



APPROVER	C. C. FIG.	
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FIG. 23

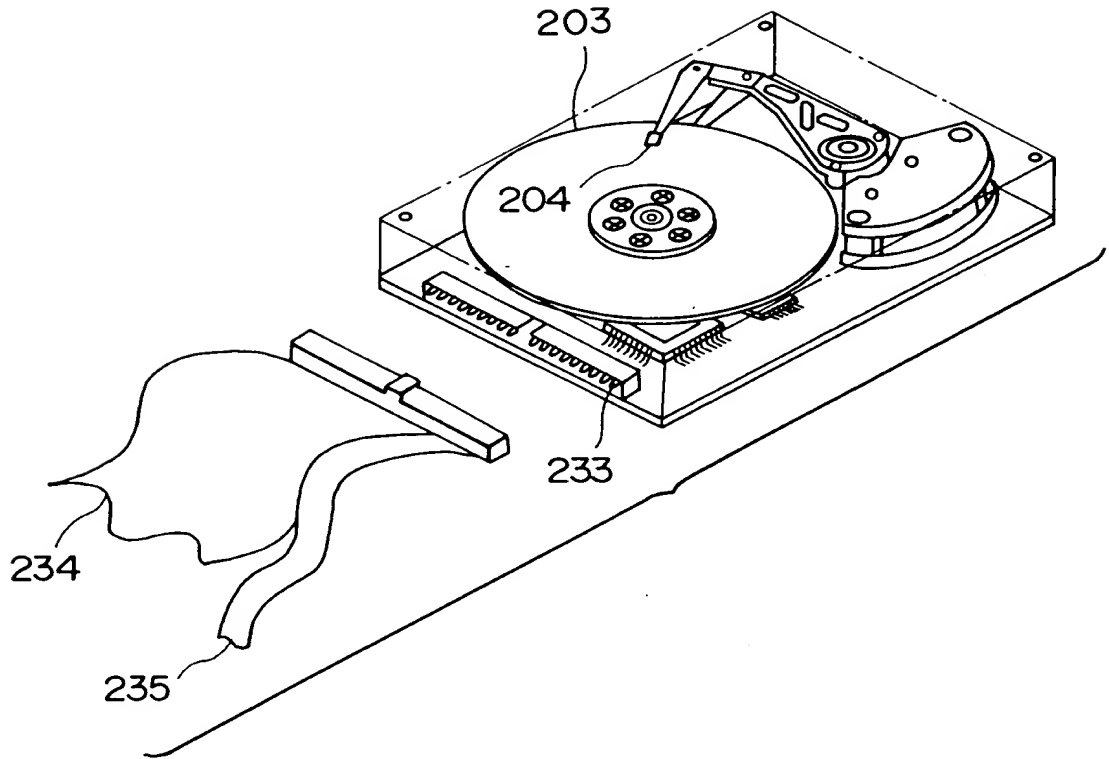
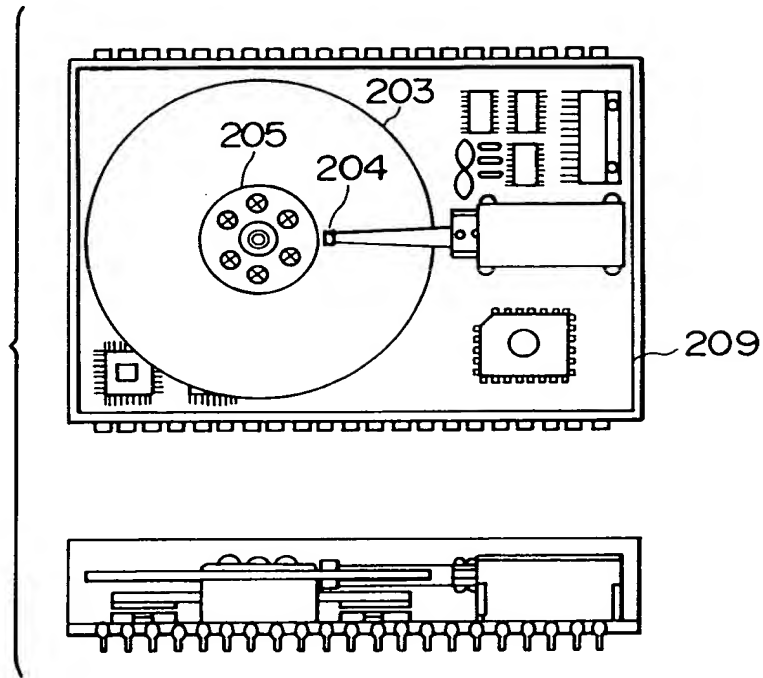


FIG. 23

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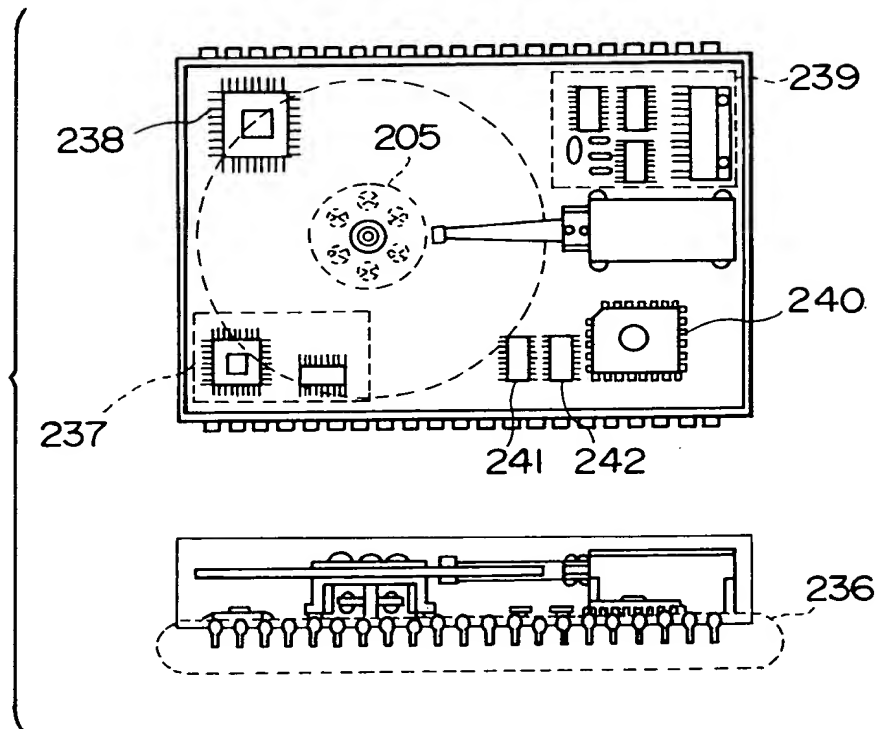
FIG. 24



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APPROVER	C. S. FIG.	
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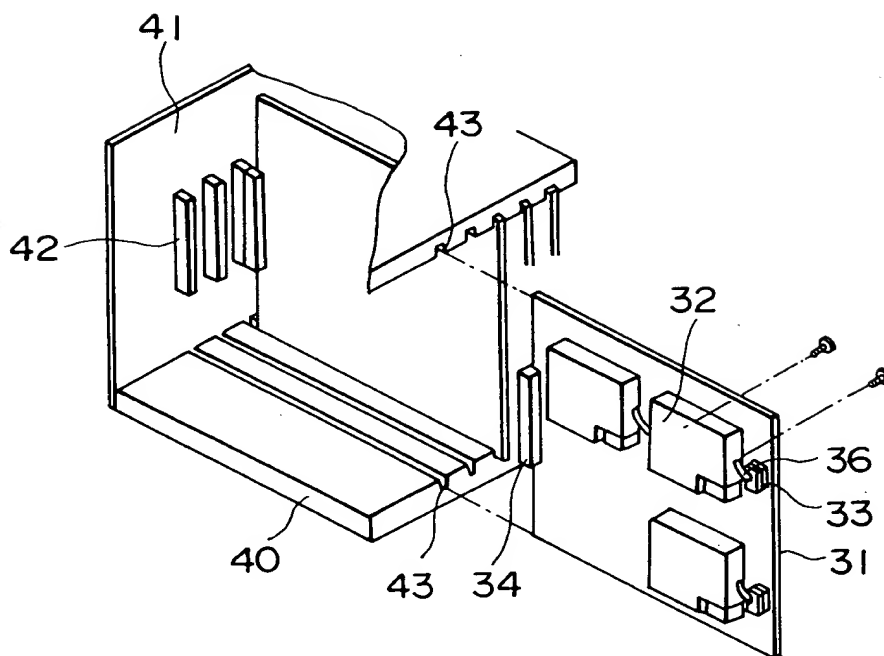
FIG. 25



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APPROVER	O. C. FIG.	
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FIG. 26
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